In the Claims:

Following is a complete listing of the claims pending in the application, as amended:

1. Canceled

2. Canceled

3. Canceled

4. Canceled

5. Canceled

6. Canceled

7. Canceled

8. Canceled

9. Canceled

10. Canceled

11. (New) An apparatus for electroplating a substrate comprising:

an electroplating bath;

an anode disposed in electrical contact with said electroplating bath;

a substrate support adapted to hold said substrate in contact with said electroplating bath during electroplating of at least one surface of said substrate;

a plurality of electrodes disposed to conduct electroplating current to said at least one surface of said substrate during electroplating;

a first current control system adapted to control the electroplating current flowing through a first electrode of said plurality of electrodes to said at least one surface; and

a second current control system adapted to control the electroplating current flowing through a second electrode of said plurality of electrodes to said at least one surface, electroplating current provided to said first and second electrodes being independently controllable by said first and second current control systems, respectively.

12. (New) The apparatus of claim 11 wherein said first electrode is formed as a discrete finger contact having a first end connected to said first current control system and a second end adapted to make electrical contact with a discrete portion of said substrate.

13. (New) The apparatus of claim 11 wherein said first current control system comprises a central processing unit, said first current control system further comprising a current control circuit associated with said first electrode of said plurality of electrodes, said current control circuit comprising:

a current monitor adapted to measure the current flow through said first electrode and provide an output signal indicative of the measured current flow, said central processing unit being responsive to an output signal of said current monitor to generate a current adjustment signal; and

a current drive circuit responsive to said current adjustment signal from said central processing unit to adjust said current flow through said first electrode whereby said current flow is driven to a target current value.

14. (New) The apparatus of claim 11 wherein said first current control system comprises:

at least one current source;

a current control circuit associated with said first electrode of said plurality of electrodes, said current control circuit including

at least one variable resistance element connected to conduct electrical current between the at least one current source and said first electrode ;

a resistance adjustment circuit connected to set the resistance of said at least one variable resistance element.

15. (New) The apparatus of claim 14 wherein said at least one variable resistance element comprises a plurality of fixed resistors disposed for selective interconnection with one another.

16. (New) The apparatus of claim 15 wherein said resistance adjustment circuit selectively interconnects said plurality of fixed resistors in an arrangement to reach a target resistance value.

17. (New) The apparatus of claim 16 wherein said first current control system comprises a central processing unit and wherein said resistance adjustment circuit comprises:

a data latch adapted to receive binary data generated by said central processing unit and to provide a plurality of binary output signals corresponding to said binary data;

a plurality of individual switching devices responsive to said binary output signals of said data latch to interconnect one or more of said plurality of fixed resistors in a resistive circuit arrangement to reach said target resistance value.

18. (New) The apparatus of claim 17 wherein each of said plurality of individual switching devices comprises a field effect transistor having a terminal connected to a respective fixed resistor, said field effect transistor being driven as a switch in response to a respective binary output signal of said data latch.

19. (New) The apparatus of claim 16 and further comprising a feedback circuit connected to monitor current flow through said variable

resistance element, said target resistance value being a function of said monitored current flow.

20. (New) The apparatus of claim 16 wherein said plurality of fixed resistors are disposed for selective parallel interconnection with one another.

21. (New) The apparatus of claim 20 wherein said first current control system comprises a central processing unit and wherein said resistance adjustment circuit comprises:

a data latch adapted to receive binary data generated by said central processing unit and to provide a plurality of binary output signals corresponding to said binary data;

a plurality of individual switching devices responsive to said binary output signals of said data latch to interconnect one or more of said plurality of fixed resistors in a resistive circuit arrangement having said target resistance value.

22. (New) The apparatus of claim 13 wherein said current drive circuit comprises at least one field effect transistor having a gate, source and drain, said field effect transistor being biased to provide a variable resistance between said source and drain in response to variations in a drive signal provided to said gate.

23. (New) The apparatus of claim 22 wherein said current drive circuit further comprises a comparator circuit connected to provide said drive signal to said gate of said field effect transistor.

24. (New) The apparatus of claim 22 wherein said first current control system comprises a central processing unit and wherein said current drive circuit comprises:

a plating waveform generator providing a plating waveform output signal;

a bias control circuit providing a bias control signal in response to a signal received from said central processing unit;

a comparator circuit having a first input connected to receive said plating waveform output signal and a second input connected to receive said bias control signal, said comparator circuit generating a differential output signal responsive to said signals at said first and second inputs, said differential output signal being provided to said gate of said field effect transistor.

25. (New) An apparatus for electroplating a substrate comprising:

a head assembly including

a stator,

a rotor disposed for rotation with respect to said stator, said rotor having a substrate support adapted to hold said substrate, said substrate support having a plurality of electrodes disposed to conduct

electroplating current to at least one surface of said substrate during electroplating;

a base assembly including

an electroplating bath,

an anode disposed in electrical contact with said electroplating bath;

said head assembly and said base assembly being movable relative to one another between a substrate loading position and a substrate processing position;

a first current control system adapted to control the electroplating current flowing through a first electrode of said plurality of electrodes;

a second current control system adapted to control the electroplating current flowing through a second electrode of said plurality of electrodes, current provided to said first and second electrodes being independently controllable by said first and second current control systems, respectively.

26. (New) The apparatus of claim 25 wherein said first electrode is formed as a discrete finger contact having a first end connected to said first current control system and a second end adapted to make electrical contact with a discrete portion of said substrate.

27. (New) The apparatus of claim 25 wherein said first current control system comprises a central processing unit, said first current control system further comprising a current control circuit

associated with said first electrode of said plurality of electrode contacts, said current control circuit comprising:

a current monitor adapted to measure the current flow through said first electrode and generating an output signal indicative of the measured current flow, said central processing unit being responsive to said output signal of said current monitor to generate a current adjustment signal; and

a current drive circuit responsive to the current adjustment signal from the central processing unit to adjust the current flow through said first electrode whereby said current flow is driven to a target current value.

28. (New) The apparatus of claim 25 wherein said first current control system comprises:

at least one current source;

a current control circuit associated with said first electrode of said plurality of electrodes, said current control circuit including

at least one variable resistance element connected to conduct electrical current between the at least one current source and said first electrode;

a resistance adjustment circuit connected to set the resistance of said at least one variable resistance element.

29. (New) The apparatus of claim 28 wherein said at least one variable resistance element comprises a plurality of fixed resistors disposed for selective interconnection with one another.

30. (New) The apparatus of claim 29 wherein said resistance adjustment circuit selectively interconnects said plurality of fixed resistors in an arrangement to reach a target resistance value.

31. (New) The apparatus of claim 30 wherein said first current control system comprises a central processing unit and wherein said resistance adjustment circuit comprises:

a data latch adapted to receive binary data generated by said central processing unit and to provide a plurality of binary output signals corresponding to said binary data;

a plurality of individual switching devices responsive to said binary output signals of said data latch to interconnect one or more of said plurality of fixed resistors in a resistive circuit arrangement to reach said target resistance value.

32. (New) The apparatus of claim 31 wherein each of said plurality of individual switching devices comprises a field effect transistor having a terminal connected to a respective fixed resistor, said field effect transistor being driven as a switch in response to a respective binary output signal of said data latch.

33. (New) The apparatus of claim 30 and further comprising a feedback circuit connected to monitor current flow through said variable

resistance element, said target resistance value being a function of said monitored current flow.

34. (New) The apparatus of claim 30 wherein said plurality of fixed resistors are disposed for selective parallel interconnection with one another.

35. (New) The apparatus of claim 34 wherein said first current control system comprises a central processing unit and wherein said resistance adjustment circuit comprises:

a data latch adapted to receive binary data generated by said central processing unit and to provide a plurality of binary output signals corresponding to said binary data;

a plurality of individual switching devices responsive to said binary output signals of said data latch to interconnect one or more of said plurality of fixed resistors in a resistive circuit arrangement having said target resistance value.

36. (New) The apparatus of claim 27 wherein said current drive circuit comprises at least one field effect transistor having a gate, source and drain, said field effect transistor being biased to provide a variable resistance between said source and drain in response to variations in a drive signal provided to said gate.

37. (New) The apparatus of claim 36 wherein said current drive circuit further comprises a comparator circuit connected to provide said drive signal to said gate of said field effect transistor.

38. (New) The apparatus of claim 36 wherein said current drive circuit comprises:

a plating waveform generator providing a plating waveform output signal;

a bias control circuit providing a bias control signal in response to a signal received from said central processing unit;

a comparator circuit having a first input connected to receive said plating waveform output signal and a second input connected to receive said bias control signal, said comparator generating a differential output signal responsive to said signals at said first and second inputs, said differential output signal being provided to said gate of said field effect transistor.

39. (New) A circuit adapted to control electrical current flow through a plurality of electrodes to a surface of a substrate in an electroplating apparatus, the circuit comprising:

at least one current source;

a first variable resistance element associated with a first electrode of said plurality of electrodes, said first variable resistance element being connected to conduct electrical current from the at least one current source and through the first electrode ;

a first resistance adjustment circuit connected to set the resistance of said first variable resistance element;

a second variable resistance element associated with a second electrode of said plurality of electrodes, said second variable resistance element being connected to conduct electrical current from the at least one current source and through the second contact;

a second resistance adjustment circuit connected to set the resistance of said second variable resistance element.

40. (New) A circuit as claimed in claim 39 wherein said first variable resistance element comprises a plurality of fixed resistors disposed for selective interconnection with one another.

41. (New) A circuit as claimed in claim 40 wherein said first resistance adjustment circuit selectively interconnects said plurality of fixed resistors in an arrangement to reach a target resistance value.

42. (New) A circuit as claimed in claim 41 and further comprising a feedback circuit connected to monitor current flow through said first variable resistance element, said target resistance value being a function of said monitored current flow.

43. (New) A circuit as claimed in claim 40 wherein said plurality of fixed resistors are disposed for selective parallel interconnection with one another.

44. (New) A circuit as claimed in claim 41 wherein said circuit further comprises a central processing unit and wherein said first resistance adjustment circuit comprises:

a data latch adapted to receive binary data generated by said central processing unit and to provide a plurality of binary output signals corresponding to said binary data;

a plurality of individual switching devices responsive to said binary output signals of said data latch to interconnect one or more of said plurality of fixed resistors in a resistive circuit arrangement having said target resistance value.

45. (New) A circuit as claimed in claim 44 wherein each of the plurality of individual switching devices comprises a field effect transistor having a terminal connected to a respective fixed resistor, said field effect transistor being driven as a switch in response to a respective binary output signal of said data latch.